O.P.Code: 16EC408	R16	H.T.No.									

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR

(AUTONOMOUS)

B.Tech II Year II Semester Supplementary Examinations May/June-2024

COMPUTER ORGANIZATION AND ARCHITECTURE

(Electronics & Communication Engineering)

Time: 3 Hours **Max. Marks: 60**

(Answer all Five Units **5 x 12 = 60** Marks)

		UNIT-I			
1	a	Sketch the internal organization of CPU out with its functionalities and block diagram.	CO1	L5	8M
	b	Write about hierarchy of buses, bus signals and its functionalities.	CO1	L3	4M
		OR			
2	a	Identify the crucial features to design the instruction set architecture for a specific purpose processor?	CO1	L1	6M
	b	Describe the Instruction set Architecture of simple computer.	CO1	L4	6M
		UNIT-II			
3	a	Illustrate the basic requirements for Input and Output communication using a terminal unit such as keyboard and printer.	CO1	L2	3M
	b	Tabulate the Input-Output Instructions using register transfer notations?	CO1	L5	9M
		OR			
4	a	Design hardware for signed magnitude addition and subtraction?	CO1	L6	6M
	b	Explain the process for signed magnitude addition and subtraction with flow chart.	CO1	L3	6M
		UNIT-III			
5	a	Design a 4-bit ALU which performs arithmetic, Logical and shift operations.	CO2	L6	6M
	b	write about hardware organization of micro programmed control unit.	CO2	L3	6M
		OR			
6	a	Demonstrate the general configuration of Micro programmed Control unit with a neat block diagram.	CO2	L2	4M
	b	Explain about address sequencing in control memory with neat diagrams?	CO2	L1	8M
		UNIT-IV			
7	a	Write about Auxiliary memory devices.	CO3	L3	3M
	b	Explain the mechanism involved in Magnetic Disks and Magnetic Tapes	CO3	L1	9M
		OR			
8		Classify and describe the possible modes of data transfer to and from peripherals with examples.	CO3	L3	12M
		UNIT-V			
9	a	Differentiate tightly coupled and loosely coupled multiprocessors.	CO3	L2	4M
	b	Write about Time shared common bus and multiport memory.	CO3	L3	8M
		OR			
10	a	Demonstrate the pipeline organisation for following example Ai*Bi+Ci for i =1,2,3,.....	CO3	L2	8M
	b	Implement a simple pipeline unit for floating addition and subtraction.	CO3	L6	4M

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